proceeds to a block 504. If IXS1 and IYS/D+1 are the same register, flow proceeds to a conditional block 512 where DDC 108 determines if IY has a valid destination. If it does not have a valid destination, there is no dependency and flow proceeds to block 504. If IY does have a valid destination, flow proceeds to a conditional block 514 where DDC 108 determines if IXS1 has a valid source register. Again, if no valid source register is detected there is no dependency, and flow proceeds to a block 504. If a valid source register is detected, DDC 108 has determined that there is a dependency between IXS1 and IYX/D, as shown at a block 516.

[0079] A more detailed discussion of data dependency checking is found in commonly owned, copending application Ser. No. 07/860,718, the disclosure of which is incorporated herein by reference. now US Patent 5,371,684, wp 06/22/94

[0080] Because it is possible that an instruction might get one of its inputs from a register that was written to by several other instructions, the present invention must choose which one is the real dependency. For example, if instructions 2 and 5 write to register 4 and instruction 7 reads register 4, then instruction 7 has two possible dependencies. In this case, it is assumed that since instruction 5 came after instruction 2 in the program, the programmer intended instruction 7 to use instruction 5's result and not instruction 2's. So, if an instruction can be dependent on several previous instructions, RRC 112 will consider it to be dependent on the highest numbered previous instruction.

[0081] Once TAL 122 has determined where the real dependencies are, it must locate the inputs for each instruction. In a preferred embodiment of the present invention, the inputs can come from the actual register file or an array of temporary buffers 116. RRC 112 assumes that if an instruction has no dependencies, its inputs are all in the register file. In this case, RRC 112 passes the IXS1, IXS2 and IXS/D addresses that came from IFIFO 102 to the register file. If an instruction has a dependency, then RRC 112 assumes that the data is in temporary buffers 116. Since RRC 112 knows which previous instruction each instruction depends on, and since each instruction always writes to the same place